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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/632,822	08/04/2003	Yoshinori Matsubara	241160US2S	9208
22850	7590	02/16/2006	EXAMINER	
OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C. 1940 DUKE STREET ALEXANDRIA, VA 22314			CLARK, SHEILA V	
			ART UNIT	PAPER NUMBER
			2823	

DATE MAILED: 02/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.		Applicant(s)	
	10/632,822		MATSUBARA, YOSHINORI	
	Examiner		Art Unit	
	S. V. Clark		2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 10-28-05.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 7-9 and 11 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 7-9 and 11 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chua et al

Chua et al shows in for example figures 3A-3F a first layer 302 at least two (i.e. plurality) of test elements 304 (right two in the figures) arranged in said layer and second layer 310 is shown in figure 3C and 3D is shown different from the first layer with a first surface adhered to the first layer and an opening portion 312 is shown in the second surface of the second layer with a plurality of first pads 314 arranged in the second layer and connected to the first test elements. Figure 3D shows said pads being exposed from the opening. A plurality of second test elements 304 (left two in the figures) arranged in the first layer and are shown electrically insulated from the first pads. The second test elements are shown arranged in the first layer below the pads. Col. 3, lines 45-48 and col.8, lines 52-55 teaches that said chips may be of a variety (i.e. memory controller, memory chips, logic chips, etc.) and therefore may be of differing types and a connecting member 320 is shown electrically connected to the second test elements. Said connecting member is shown in layer 316 and therefore does not exist in the second layer 310.

As the claims have not defined "test elements", said elements have been broadly interpreted to mean elements that may be tested. The chips taught by Chua et al are deemed to obviously be elements that may be tested and therefore obviously test elements.

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chua et al

Chua et al shows in for example figures 3A-3F a first layer 302 at least two (i.e. plurality) of test elements 304 (right two in the figures) arranged in said layer and second layer 310 is shown in figure 3C and 3D is shown different from the first layer with a first surface adhered to the first layer and an opening portion 312 is shown in the second surface of the second layer with a plurality of first pads 314 arranged in the second layer and connected to the first test elements. Figure 3D shows said pads being exposed from the opening. A plurality of second test elements 304 (left two in the figures) arranged in the first layer and are shown electrically insulated from the first pads. The first test elements are also shown located in the first y line location and the second test elements are located in a second y line location parallel and therefore different from the first. A connecting member 320 is shown electrically connected to the second test elements. Said connecting member is shown in layer 316 and therefore does not exist in the second layer 310.

As the claim has not specifically characterized "test elements," said elements have been broadly interpreted to mean elements that may be tested. The chips taught by Chua et al are deemed to obviously be elements that may be tested and therefore obviously test elements. Further as the claim has also failed to characterize "line" said line interpreted broadly has not been viewed as being planer.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chua et al

Chua et al shows in for example figures 3A-3F a first layer 302 at least two (i.e. plurality) of test elements 304 (right two in the figures) arranged in said layer and second layer 310 is shown in figure 3C and 3D is shown different from the first layer with a first surface adhered to the first layer and an opening portion 312 is shown in the second surface of the second layer with a plurality of first pads 314 arranged in the second layer and connected to the first test elements. Figure 3D shows said pads being exposed from the opening. A plurality of second test elements 304 (left two in the figures) arranged in the first layer and are shown electrically insulated from the first pads. Col. 3, lines 45-48 and col.8, lines 52-55 teach that said chips may be of a variety (i.e. memory controller, memory chips, logic chips, etc.) and therefore different. The second test elements are shown arranged in the first layer below the pads.

As the claims has not specifically characterized "test elements" said elements have been broadly interpreted to mean elements that may be tested. The chips taught

by Chua et al are deemed to obviously be elements that may be tested and therefore obviously test elements.

A third layer 316 is shown adhered to the second layer and having bumps 320 therein and arranged on part of the pads. First connection members in the form of chip signal pads (not labeled) but are inherently formed on the chip and are exposed in signal connection opening 306. And a second connection member 308 is shown in the second layer connected to said pads and the first connection member.

A plurality of second test elements 304 (left two in the figures) are arranged in the first layer and are shown electrically insulated from the first pads. A connecting member 320 is shown electrically connected to the second test elements. Said connecting member is shown in layer 316 and therefore does not exist in the second layer 310.

Chua et al suggests that the invention may be modified to include additional connection members (col.8, lines 25 to 32) as well the use of other connective bumps in the third layer (col. 8, line 38-39). It would have been therefore obvious to one having ordinary skill in this art that the invention of Chua et al may be modified to include a third connection member in the third layer as suggested in the modifications disclosed by Chua et al where multiple layer bumps structures, multilayer and laminated wiring connections which would all render a third connection member and would be well known to a workman having ordinary skill in this art.

Chua et al also teaches that said bumps may be used for testing.


Claims 7, 8, 9, 11 are rejected.

Applicant's arguments filed 10-28-05 have been fully considered but they are not persuasive. The amendments to the claims continue to be taught by the prior art utilized in the rejection. Applicant continues to utilize terms that may have broad meanings such as "connecting member". Though applicant's arguments identify said connecting member as 308 in the Chua reference, a "connecting member" is not limited to any one type of interconnection. Component 320 is also a connection member as identified in the rejection. Further contrary to applicant's arguments it is not clear where Chua shows that a connecting member 308 is connected to all first and second test members.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication should be directed to at telephone number (571) 272-1725.


S. V. Clark
Primary Examiner
Art Unit 2823

January 10, 2006